REMARKS

Claims 1-21 are pending in the present application. Claims 1 and 9 are independent claims.

35 U.S.C. §§ 102(b) & 103 REJECTIONS

Claims 1-7 and 9-19 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshida et al. (U.S. Patent No. 5,734,455). Claims 8 and 20-21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshida et al. These rejections, insofar as they pertain to the presently pending claims, are respectfully traversed.

Regarding independent claims 1 and 9, the Examiner alleges that Yoshida et al. teaches a light leakage prevention film of Applicants' invention because Yoshida et al. discloses a reflective film 22 as shown in Fig. 1, or a capacitor electrode 222 or 323 as shown in Figs. 5 and 9. However, each of the reflective film 22, the capacitor electrode 222 and the capacitor electrode 323 in Yoshida et al. is located in the array region, and not in the array peripheral region. Specifically, each of the layers 22, 222 and 323 is disposed on a rear surface side of a pixel electrode 13 or 213. Please see, e.g., column 7, lines 66-67 of Yoshida et al. In other words, Yoshida et al.'s reflective film 22 or capacitor electrode 222, 323 is disposed in the array region where the pixel electrodes are.

In clear contrast, in Applicants' invention, the light leakage prevention film is formed between the gate lines and/or data lines of the array peripheral region, where the array peripheral region excludes pixel electrodes. This feature is nowhere found in Yoshida et al.

Furthermore, it would not have been obvious to modify Yoshida et al.'s device to move the location of the reflective film 22 or capacitor electrode 222 or 323, because their relationship with respect to the pixel electrode is important and should be preserved so that the reflective film or the capacitor electrode can function as part of a capacitor. Please see, e.g., column 8, lines 10-14 of Yoshida et al.

Therefore, Yoshida et al. does not teach or suggest, *inter alia:*

> a light leakage prevention film formed between the gate lines and/or data lines of the array peripheral region..., the array peripheral region excluding pixel electrodes

as recited in independent claim 1; and

> forming a light leakage prevention film between the gate lines and/or the data lines of the array peripheral region to prevent light leakage, the array peripheral region excluding pixel electrodes

as recited in independent claim 9.

Accordingly, independent claims 1 and 9 and their dependent claims (due to their dependency) are patentable over the applied reference, and reconsideration and withdrawal of the rejections based on these reasons is respectfully requested.

CONCLUSION

For the foregoing reasons and in view of the above clarifying amendments, Applicants respectfully request the Examiner to reconsider and withdraw all of the objections and rejections of record, and earnestly solicit an early issuance of a Notice of Allowance.

Should there be any outstanding matters which need to be resolved in the present application, the Examiner is respectfully requested to contact Esther H. Chong (Registration No. 40,953) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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Enclosure: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims

1. (Amended) A display panel including a first substrate having an array region and an array peripheral region, and a second substrate having a black matrix, the display panel comprising:

a plurality of gate lines on the first substrate;

a gate insulating film on the first substrate including the gate lines;

a plurality of data lines arranged to cross the gate lines, for defining a pixel region on the array region; and

a light leakage prevention film formed between the gate lines and/or data lines of the array peripheral region, for preventing light leakage, the array peripheral region excluding pixel electrodes.

2. (Amended) The display panel as claimed in claim 1, further comprising:

a TFT and a pixel electrode formed in each pixel region located in the array region.

9. (Amended) A method for manufacturing a display panel including a first substrate having an array region and an array peripheral region, and a second substrate having a black matrix, the method comprising the steps of:

forming a plurality of gate lines on the first substrate;

forming a gate insulating film on the first substrate including the gate lines;

forming a plurality of data lines to cross the gate lines and define a pixel region on the array region; and

forming a light leakage prevention film between the gate lines and/or the data lines of the array peripheral region to prevent light leakage, the array peripheral region excluding pixel electrodes.

10. (Amended) The method [display panel] according to claim 9, further comprising the steps of:

forming a TFT at a crossing point of a corresponding one of the gate lines and a corresponding one of the data lines;

forming a passivation film on the first substrate including the TFT; and

forming, in the array region, a pixel electrode coupled with the TFT on the passivation film.